

Figure 1

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Order latches in the circuit in the bottom-up order (from inputs to the outputs):

Let  $l_1, l_2, \dots, l_n$  be thus ordered list of latches (assumed is the data signal of  $l_1$  and  $c_1$  is its clock signal)

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For each latch  $l_i$  in the above order, compute its TBED,  $\text{tbred}(l_i)$ , as follows:

- compute the TBED of its data,  $\text{tbred}(d_i)$  (item 9 of the pseudo-algorithm)
- compute the TBED of its clock,  $\text{tbred}(c_i)$  (item 10 of the pseudo-algorithm)
- compute  $\text{res}_i =$  the restriction of  $\text{tbred}(\text{data}_i)$  over  $\text{tbred}(c_i)$  (item 10 of the pseudo-alg)

The TBED of latch  $l_i$  is computed by:  $\text{tbred}(l_i) = \text{shift}(\text{res}_i, \text{tbred}(c_i))$  (item 11 of the pseudo-alg)

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Compute the TBED of the output (item 20 of the pseudo algorithm)

Figure 2

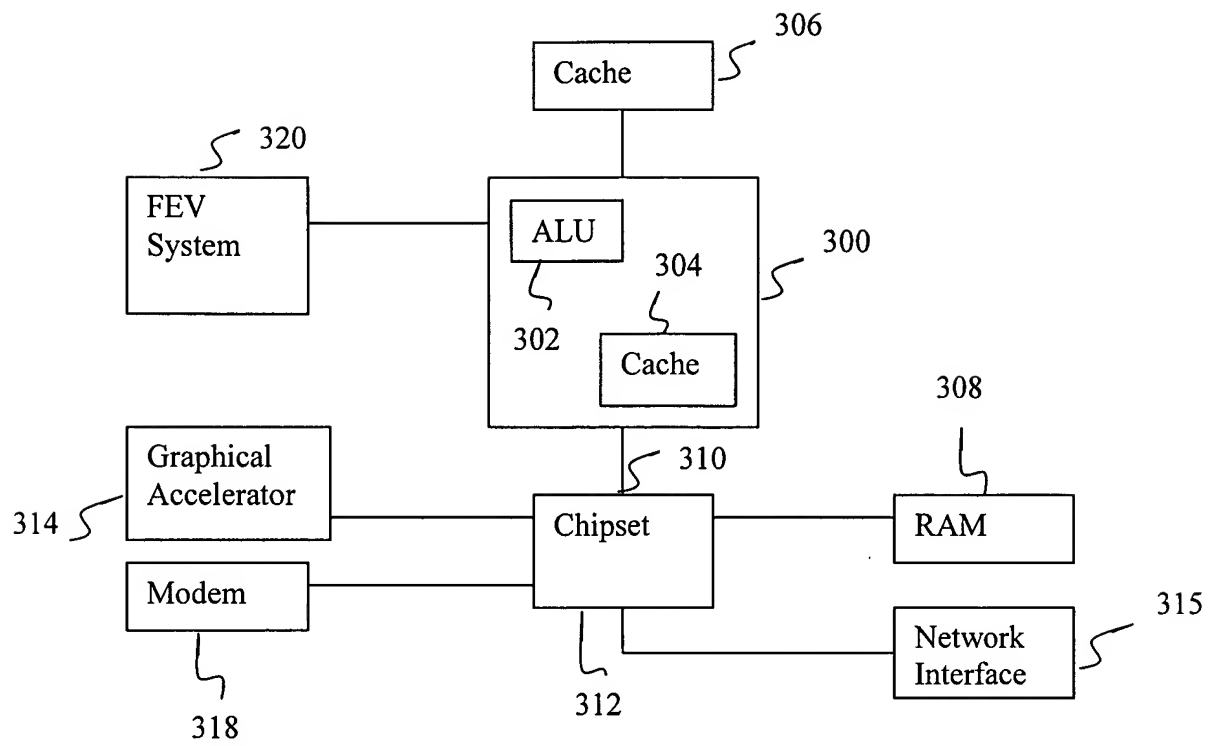


Figure 3